## CLAIMS

The current set of claims are reproduced in the following claim listing. No claims have been amended, canceled, or added.

1. (Previously presented) A system comprising:

a bus having a plurality of lines;

a first device having a first transmitter to transmit first signals in a first frequency band over one line of the bus and having a receiver to receive second signals in a second frequency band over the one line of the bus while first signals are transmitted over the one line of the bus; and

a second device to communicate with the first device over the bus, the second device having a second transmitter to transmit second signals in the second frequency band over the one line of the bus,

wherein the first frequency band and the second frequency band occupy different portions of a frequency spectrum.

2. (Previously presented) The system of claim 1 wherein the first transmitter includes a filter having a cutoff frequency to define at least in part the first frequency band.

3. (Previously presented) The system of claim 1 wherein the first transmitter includes an encoder to define at least in part the first frequency band.

4. (Previously presented) The system of claim 3 wherein the encoder has a defined run length.

5. (Previously presented) The system of claim 3 wherein the encoder comprises a combinational logic table.

6. (Previously presented) The system of claim 1 wherein the first transmitter and the receiver are part of a single chip.

7. (Original) The system of claim 1 wherein the first frequency band and the second frequency band are fixed.

8. (Previously presented) The system of claim 1 comprising a band setting unit to set the first frequency band and the second frequency band in response to an input signal.

9. (Previously presented) The system of claim 8 comprising a user selection device to generate the input signal.

10. (Previously presented) The system of claim 8 comprising a first arbitration module and a second arbitration module to arbitrate between one another to generate the input signal.

11. (Previously presented) The system of claim 1 wherein the first transmitter and the receiver are associated with a microprocessor.

12. (Previously presented) The system of claim 1 wherein the first transmitter and the receiver are associated with a memory storage device.

13. (Previously presented) The system of claim 1 wherein the first transmitter and the receiver are associated with a chipset.

14. (Previously presented) The system of claim 1 wherein:
the first transmitter includes a first output connected to the one line of the bus;
the second transmitter includes a second output connected to the one line of the bus; and
the receiver includes an input connected to the one line of the bus.

15. (Previously presented) A device comprising:

a transmitter to transmit first signals in a first frequency band over one of a plurality of lines of a bus over which the device is to communicate with another device;

a receiver to receive second signals in a second frequency band over the one line of the bus while first signals are transmitted over the one line of the bus,

wherein the first frequency band and the second frequency band occupy different portions of a frequency spectrum; and

a functional portion to transmit signals using the transmitter and to receive signals using the receiver.

16. (Previously presented) The device of claim 15 wherein the transmitter includes a filter having a cutoff frequency to define at least in part the first frequency band.

17. (Previously presented) The device of claim 15 wherein the transmitter includes an encoder to define at least in part the first frequency band.

18. (Previously presented) The device of claim 15 wherein the first frequency band and the second frequency band are fixed.

19-26. (Canceled).

27. (Previously presented) A method comprising:

transmitting by a first device first signals in a first frequency band over one of a plurality of lines of a bus over which the first device is to communicate with a second device; and

receiving by the first device second signals in a second frequency band over the one line of the bus while first signals are transmitted over the one line of the bus,

wherein the first frequency band and the second frequency band occupy different portions of a frequency spectrum.

28. (Previously presented) The method of claim 27 wherein transmitting first signals includes encoding an output to form a first signal in the first frequency band.

29. (Previously presented) The method of claim 28 wherein transmitting first signals includes encoding an output to form a first signal with a defined run length.

30. (Previously presented) The method of claim 27 comprising setting the first frequency band and the second frequency band.

31. (Previously presented) The method of claim 30 wherein the setting comprises arbitrating between the first and second devices.

32. (Previously presented) The method of claim 30 wherein the setting comprises setting the first frequency band by a user.

33. (Previously presented) The method of claim 27 wherein the second device comprises memory and wherein the method comprises:

transmitting a first signal to request data from the memory; and

receiving a second signal to receive requested data from the memory.

34. (Previously presented) The system of claim 1 wherein the second device has a receiver to receive first signals over the one line of the bus while second signals are transmitted over the one line of the bus.

35. (Previously presented) The device of claim 15, wherein the functional portion is a processor.

36. (Previously presented) The device of claim 15, wherein the functional portion is memory.

37. (Previously presented) The device of claim 15, wherein the functional portion is a controller for a chipset.

38. (Previously presented) The device of claim 15, wherein the transmitter, receiver, and functional portion are part of a single chip.

39. (Previously presented) The device of claim 17, wherein the encoder has a defined run length.

40. (Previously presented) The device of claim 17, wherein the encoder comprises a combinational logic table.

41. (Previously presented) The device of claim 15, comprising an arbitration module to set the first frequency band.